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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,431	10/22/2003	Dieter Dornisch	0150141	8402

25700 7590 07/27/2004

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,431	DORNISCH ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng et al. (U.S. Patent No. 6,693,321) in view of Applicant's admitted prior art as disclosed in figure 2 and its description on pages 7-9 of the instant application. With regard to Claim 1, Zheng discloses a high-k dielectric stack (24) situated between an upper electrode (32) and a lower electrode (18) of a capacitor structure, said high-k dielectric stack comprising: a first high-k dielectric (column 7, lines 22-23) layer (26), said first high-k dielectric layer having a first dielectric constant; an intermediate dielectric layer (28) situated on said first high-k dielectric layer (26), said

intermediate dielectric layer (28) having a second dielectric constant (column 7, lines 25-28); a second high-k dielectric (column 7, lines 31-32) layer (30) situated on said intermediate dielectric layer (28), said second high-k dielectric layer (30) having a third dielectric constant (column 7, lines 31-34); wherein said second dielectric constant is not greater than said first dielectric constant and said third dielectric constant (column 7, lines 25-28). See also figure 1.

However, Zheng fails to teach that the high-k dielectric stack is situated between an upper electrode and a lower electrode of a MIM capacitor. Applicant's admitted prior art, as disclosed in figure 2, discloses a MIM capacitor (102) including a high-k dielectric stack (122) situated between an upper electrode (114) and a lower electrode (106). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the high-k dielectric stack structure as taught by Zheng in a MIM capacitor structure as disclosed by Applicant's admitted prior art, in order to allow further scaling of the capacitor structure device and improve its manufacturing process (see Zheng, column 4, lines 14-20).

With regard to Claim 2, a further difference between the claimed invention and Zheng is the limitation of *first and second cladding layers, said first cladding layer being situated underneath said first high-k dielectric layer and said second cladding layer being situated on said second high-k dielectric layer.* However, Applicant's admitted prior art, as disclosed in figure 2, discloses first (108) and second (112) cladding layers, wherein said first cladding layer (108) is situated underneath a high-k dielectric layer (110) and said second cladding layer (112) is situated on said high-k dielectric layer (110). Therefore, it would have been obvious to someone

with ordinary skill in the art, at the time of the invention, to include first and second cladding layers in a high-k dielectric stack structure as taught by Zheng.

With regard to Claim 3, Zheng discloses a second dielectric constant that is less than said first dielectric constant and said third dielectric constant (column 7, lines 25-28).

With regard to Claim 4, Zheng discloses an intermediate dielectric layer (28) that comprises Al_2O_3 (column 7, lines 25-27 and column 8, lines 11-51).

With regard to Claim 5, Zheng discloses an intermediate dielectric layer (28), which has a thickness between approximately 5.0 Angstroms and approximately 70.0 Angstroms (column 7, lines 29-31).

With regard to Claim 6, a further difference between the claimed invention and Zheng is the limitation of a *first cladding layer is situated on said lower electrode and said upper electrode is situated on said second cladding layer*. However, Applicant's admitted prior art, as disclosed in figure 2, discloses a first cladding layer (108) is situated on a lower electrode (106) and an upper electrode (114) is situated on a second cladding layer (112). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include first and second cladding layers in a high-k dielectric stack structure as taught by Zheng.

With regard to Claim 7, a further difference between the claimed invention and Zheng is the limitation of a *lower electrode comprising Ti/TiN and an upper electrode comprising TiN.* However, Applicant's admitted prior art, as disclosed in figure 2, discloses a lower electrode (106) comprising TiN and an upper electrode (114) comprising TiN. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include a lower electrode comprising Ti/TiN and an upper electrode comprising TiN in combination with a high-k dielectric stack as taught by Zheng, in order to provide a capacitor which uses electrode materials known in the semiconductor for their reliability.

With regard to Claim 8, Zheng discloses first (26) and second (30) high-k dielectric layers selected from the group consisting of HfO_2 and Ta_2O_5 (column 7, lines 23-24; column 7, lines 31-33 and column 8, lines 14-51).

With regard to Claim 9, Zheng discloses a method for fabricating a MIM capacitor in a semiconductor die, comprising the steps of: forming a lower electrode (18) of a capacitor structure, forming a first high-k dielectric (column 7, lines 22-23) layer (26) over said lower electrode (18), said first high-k dielectric layer having a first dielectric constant; forming an intermediate dielectric layer (28) on said first high-k dielectric layer (26), said intermediate dielectric layer (28) having a second dielectric constant (column 7, lines 25-28); forming a second high-k dielectric (column 7, lines 31-32) layer (30) on said intermediate dielectric layer (28), said second high-k dielectric layer (30) having a third dielectric constant (column 7, lines 31-34); forming an upper electrode (32) of the capacitor structure over said second high-k

dielectric layer (30); wherein said second dielectric constant is not greater than said first dielectric constant and said third dielectric constant (column 7, lines 25-28). See also figure 1.

However, Zheng fails to teach that the upper electrode and the lower electrode are part of a MIM capacitor. Applicant's admitted prior art, as disclosed in figure 2, discloses a MIM capacitor (102) including a high-k dielectric stack (122) situated between an upper electrode (114) and a lower electrode (106). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include the high-k dielectric stack structure as taught by Zheng in a MIM capacitor structure including upper and lower electrodes, as disclosed by Applicant's admitted prior art, in order to allow further scaling of the capacitor structure device and improve its manufacturing process (see Zheng, column 4, lines 14-20).

With regard to Claim 10, a further difference between the claimed invention and Zheng is the limitation of *forming a first cladding layer on said lower electrode before said step of forming said first high-k dielectric layer; forming a second cladding layer on said second high-k dielectric layer after said step of forming said second high-k dielectric layer*. However, Applicant's admitted prior art, as disclosed in figure 2 and page 8, lines 2-18, discloses forming first (108) and second (112) cladding layers, wherein said first cladding layer (108) is formed on a lower electrode (106) before the step of forming high-k dielectric layer (110) and forming a second cladding layer (112) on said high-k dielectric layer (110) after said step of forming said high-k dielectric layer (110). Therefore, it would have been obvious to someone with ordinary

skill in the art, at the time of the invention, to include the step of forming first and second cladding layers in the formation of the high-k dielectric stack structure as taught by Zheng.

With regard to Claim 11, Zheng discloses a second dielectric constant that is less than said first dielectric constant and said third dielectric constant (column 7, lines 25-28).

With regard to Claim 12, Zheng discloses an intermediate dielectric layer (28) that comprises Al_2O_3 (column 7, lines 25-27 and column 8, lines 11-51).

With regard to Claim 13, Zheng discloses an intermediate dielectric layer (28), which has a thickness between approximately 5.0 Angstroms and approximately 70.0 Angstroms (column 7, lines 29-31).

With regard to Claim 14, a further difference between the claimed invention and Zheng is the limitation of a *lower electrode comprising Ti/TiN and an upper electrode comprising TiN.* However, Applicant's admitted prior art, as disclosed in figure 2, discloses a lower electrode (106) comprising TiN and an upper electrode (114) comprising TiN. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include a lower electrode comprising Ti/TiN and an upper electrode comprising TiN in combination with a high-k dielectric stack as taught by Zheng, in order to provide a capacitor which uses electrode materials known in the semiconductor for their reliability.

With regard to Claim 15, Zheng discloses first (26) and second (30) high-k dielectric layers selected from the group consisting of HfO_2 and Ta_2O_5 (column 7, lines 23-24; column 7, lines 31-33 and column 8, lines 14-51).

With regard to Claim 16, Zheng discloses a high-k dielectric stack (24) situated between an upper electrode (32) and a lower electrode (18) of a capacitor structure, said high-k dielectric stack comprising: a first high-k dielectric (column 7, lines 22-23) layer (26), said first high-k dielectric layer having a first dielectric constant; an intermediate dielectric layer (28) situated on said first high-k dielectric layer (26), said intermediate dielectric layer (28) having a second dielectric constant (column 7, lines 25-28); a second high-k dielectric (column 7, lines 31-32) layer (30) situated on said intermediate dielectric layer (28), said second high-k dielectric layer (30) having a third dielectric constant (column 7, lines 31-34); wherein said second dielectric constant is not greater than said first dielectric constant and said third dielectric constant (column 7, lines 25-28). See also figure 1.

However, Zheng fails to teach a first cladding layer situated on the lower electrode, a second cladding layer situated on the second high-k dielectric layer and that the upper electrode and the lower electrode are part of a MIM capacitor. Applicant's admitted prior art, as disclosed in figure 2, discloses first (108) and second (112) cladding layers, wherein said first cladding layer (108) is situated on a lower electrode (106) and said second cladding layer (112) is situated on said high-k dielectric layer (110). Therefore, it would have been obvious to someone with ordinary

skill in the art, at the time of the invention, to include the step of forming first and second cladding layers in the formation of the high-k dielectric stack structure as taught by Zheng.

With regard to Claim 17, Zheng discloses a second dielectric constant that is less than said first dielectric constant and said third dielectric constant (column 7, lines 25-28).

With regard to Claim 18, Zheng discloses an intermediate dielectric layer (28) that comprises Al_2O_3 (column 7, lines 25-27 and column 8, lines 11-51).

With regard to Claim 19, Zheng discloses an intermediate dielectric layer (28), which has a thickness between approximately 5.0 Angstroms and approximately 70.0 Angstroms (column 7, lines 29-31).

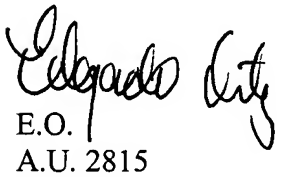
With regard to Claim 20, a further difference between the claimed invention and Zheng is the limitation of a *lower electrode comprising Ti/TiN and an upper electrode comprising TiN.* However, Applicant's admitted prior art, as disclosed in figure 2, discloses a lower electrode (106) comprising TiN and an upper electrode (114) comprising TiN. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to include a lower electrode comprising Ti/TiN and an upper electrode comprising TiN in combination with a high-k dielectric stack as taught by Zheng, in order to provide a capacitor which uses electrode materials known in the semiconductor for their reliability.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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